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10/068,492	02/05/2002	Michael J. Tsecouras	TI-33116	7292

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EXAMINER	
BHATTACHARYA, SAM	

ART UNIT	PAPER NUMBER
2687	

DATE MAILED: 06/02/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/068,492	TSECOURAS, MICHAEL J.	
	Examiner	Art Unit	
	Sam Bhattacharya	2687	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 December 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-29* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-29* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. Claims 1-5, 11-15, 18-21, 24-25, and 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent 5,341,402 to Matsushita et al. in view of Orndorff (U.S. Patent 5,640,697).

As to claim 1, Figure 7 in Matsushita shows a digital amplifier adaptive pulse frame rate frequency control system comprising:

a sample rate converter (74) (see Col. 6, lines 40-43);

a programmable controller (75) operational to generate control data bits (see Col. 6, lines 43-59); and

a system clock generator (76) operational to generate a sample rate converter master clock signal in response to the control data bits such that the sample rate converter generates output data at a sample rate determined by the control data bits (see Col. 6, lines 43-48).

However, the Matsushita reference does not disclose a programmable controller operational in response to user selected input frequency data to generate control data bits. The Orndorff reference teaches a programmable controller operational in response to user selected input frequency data to generate control data bits (see Figure 3, Col. 3, lines 9-15, Col. 5, lines 9-28, Col. 8, lines 12-16, and Col. 11, line 59 to Col. 12 line 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Matsushita to comprise a programmable

controller operational in response to user selected input frequency data to generate control data bits, as taught by Orndorff, in order to program the controller to respond to inputs for tuning.

As to claims 2, 13, and 19, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 1, 12, and 18 wherein the programmable controller comprises a data processing device selected from the group consisting of a computer, a digital signal processor (DSP), a CPU, and a micro-controller (Matsushita: see Figure 6, and Col. 5, line 62 to Col. 6, line 18. Orndorff: see Col. 5, lines 9-16).

As to claims 3, 14, and 20, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 1, 12, and 18 wherein the system clock generator comprises a frequency controller selected from the group consisting of a digital frequency synthesizer, and a programmable phase-locked loop (Matsushita: see Col. 5, lines 10-27).

As to claims 4, 15, and 21, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 1, 12, and 18 wherein the system clock generator is further operational to generate audio clock signals at the sample rate determined by the control data bits (Matsushita: see Col. 6, lines 43-48 and Figure 7. It is inherent that if the received signal is audio clock signal, then the system clock generator generates audio clock signals at the determined sample rate).

As to claims 5 and 24, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 4 and 18 wherein the system clock generator is further operational to generate sample clock signals at the sample rate determined by the control data bits (Matsushita: see Col. 6, lines 43-48 and Figure 7).

As to claim 11, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claim 1 wherein the sample rate converter comprises a digital asynchronous sample rate converter (Matsushita; "A/D converter 74" in Figure 7 and Col. 6, lines 40-43).

As to claim 12, Figure 7 in Matsushita shows a digital amplifier adaptive pulse frame rate frequency control system comprising:

a digital asynchronous sample rate converter (74) operational to generate output audio data in response to input audio data, an input audio clock and a master clock (see Col. 6, lines 40-43);

a programmable controller (75) operational to generate control data bits (see Col. 6, lines 43-59);

a decoder operational to decode the control data bits (see Col. 6, lines 43-59. It is inherent that there is a decoder in the sampling clock generator 76 to decode the control data from the microprocessor 75); and

a system clock generator (76) operational to generate the master clock in response to the decoded control data bits such that the digital asynchronous sample rate converter generates the output data at a sample rate determined by the user selected input frequency information (see Col. 6, lines 43-48).

However, the Matsushita reference does not disclose a programmable controller operational in response to user selected input frequency information to generate control data bits, wherein the input frequency information is selected from the group consisting of wireless, cellular telephone, Bluetooth, RF, IF, LCO, AM, FM, and TV band frequencies. The Orndorff

reference teaches a programmable controller operational in response to user selected input frequency information to generate control data bits, wherein the input frequency information is selected from the group consisting of wireless, cellular telephone, Bluetooth, RF, IF, LCO, AM, FM, and TV band frequencies (see Figure 3, Col. 1, lines 13-20, Col. 3, lines 9-15 and 23-30, Col. 4, lines 37-42, Col. 5, lines 9-28, Col. 5, line 44 to Col. 8, line 20, and Col. 11, line 59 to Col. 12 line 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Matsushita to comprise a programmable controller operational in response to user selected input frequency information to generate control data bits, wherein the input frequency information is selected from the group consisting of wireless, cellular telephone, Bluetooth, RF, IF, LCO, AM, FM, and TV band frequencies, as taught by Orndorff, in order to program the controller to respond to inputs for tuning.

As to claim 18, what is cited in claim 12 is applicable to this claim 18. Claim 18 is the same as claim 12, except "means" is used in placed of an element (e.g., programmable controlling means in claim 18 versus a programmable controller in claim 12).

As to claim 25, Figure 7 in Matsushita shows a method of controlling the pulse-frame rates for a digital amplifier output signal comprising the steps of:

providing a pulse-frame rate frequency control system having a programmable controller (75), a system clock generator (76), and a digital asynchronous sample rate converter (74) operational to generate output audio data at a first sample rate in response to input audio data and further in response to input audio clocks (see Col. 6, lines 40-59);

communicating the control data bits to the system clock such that the system clock generates a master clock for the digital asynchronous sample rate converter at a new sample rate and further such that the system clock generates output audio clocks at the new sample rate (see Col. 6, lines 43-59); and

adapting the digital asynchronous sample rate converter output audio data at a first sample rate to conform to the new sample rate determined by the master clock (see Col. 6, lines 40-43).

However, it does not disclose communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data. The Orndorff reference teaches communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data (see Figure 3, Col. 3, lines 9-15, Col. 5, lines 9-28, Col. 8, lines 12-16, and Col. 11, line 59 to Col. 12 line 8).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Matsushita to comprise the step of communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data, as taught by Orndorff, in order to program the controller to respond to inputs for tuning.

As to claim 28, Matsushita-Orndorff discloses the method of claim 25 wherein the step of communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data comprises the step of providing a look-up table of pulse-frame frequencies (output digital asynchronous sample

rate converter clock generator frequencies) versus station data selected from the group consisting of RF, IF, LCO, AM, FM, TV station, wireless, cellular telephone and Bluetooth frequencies, that can be accessed by the controller to determine the control data bits (Orndorff: see Figure 3, Col. 1, lines 13-20, Col. 3, lines 9-15 and 23-30, Col. 4, lines 37-42, Col. 5, lines 9-28, Col. 5, line 44 to Col. 8, line 20, and Col. 11, line 59 to Col. 12 line 8).

As to claim 29, Matsushita-Orndorff discloses the method of claim 25 wherein the step of communicating user selected input frequency data to the controller such that the controller generates control data bits determined by the user selected input frequency data comprises the step of providing an algorithm to select pulse-frame frequencies (output digital asynchronous sample rate converter clock generator frequencies) versus station data selected from the group consisting of RF, IF, LCO, AM, FM, TV station, wireless, cellular telephone and Bluetooth frequencies, that can be accessed by the controller to determine the control data bits (Orndorff: see Figure 3, Col. 1, lines 13-20, Col. 3, lines 9-15 and 23-30, Col. 4, lines 37-42, Col. 5, lines 9-28, Col. 5, line 44 to Col. 8, line 20, and Col. 11, line 59 to Col. 12 line 8).

3. Claims 6-10, 16-17, 22-23, and 26-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Matsushita et al. in view of Orndorff, and further in view of Midya et al. (U.S. Patent Application Publication 2002/0180518 A1).

As to claims 6, 16, and 22, Matsushita-Orndorff discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 4, 15, and 21. However, it does not disclose a digital amplifier responsive to the system clock generator audio clock signals and the sample rate converter output data such that the digital amplifier output switches at a pulse-

frame rate determined by the system clock generator audio clock signals and the sample rate converter output data. The Midya reference teaches a digital amplifier responsive to the system clock generator audio clock signals and the sample rate converter output data such that the digital amplifier output switches at a pulse-frame rate determined by the system clock generator audio clock signals and the sample rate converter output data (see Figure 1 and page 1, col. 2, paragraphs [0010] – [0011]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the system of Matsushita-Orndorff to further comprise a digital amplifier responsive to the system clock generator audio clock signals and the sample rate converter output data such that the digital amplifier output switches at a pulse-frame rate determined by the system clock generator audio clock signals and the sample rate converter output data, as taught by Midya, in order to provide error correction in digital amplifiers.

As to claims 7, 17, and 23, Matsushita-Orndorff-Midya discloses the digital amplifier adaptive pulse frame rate frequency control system according to claims 6, 16, and 22 wherein the digital amplifier output further switches at a pulse-frame rate to minimize interference associated with keep-out bands for frequencies related to a desired source (Midya: see page 2, col. 1, paragraph [0012]).

As to claim 8, Matsushita-Orndorff-Midya discloses the digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are associated with frequencies selected from the group consisting of AM, FM and TV band frequencies (Orndorff: see Col. 1, lines 13-15, Col. 3, lines 23-30 and Col. 4, lines 37-42).

As to claim 9, Matsushita-Orndorff-Midya discloses the digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are associated with frequencies selected from the group consisting of radio frequency (RF), intermediate frequency (IF), and Local Control Oscillator (LCO) frequencies (Orndorff: see Col. 5, line 44 to Col. 8, line 20).

As to claim 10, Matsushita-Orndorff-Midya discloses the digital amplifier adaptive pulse frame rate frequency control system according to claim 7 wherein the keep-out bands are associated with wireless communication frequencies selected from the group consisting of cellular telephone frequencies and Bluetooth frequencies (Matsushita: see Col. 1, lines 7-10 and Col. 5, lines 42-45. Orndorff: see Col. 1, lines 13-20 and Col. 13, line 28 to Col. 14, line 4).

As to claim 26, Matsushita-Orndorff discloses the method according to claim 25. However, it does not disclose the steps of: providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate. The Midya reference teaches the steps of: providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate (see Figure 1 and page 1, col. 2, paragraphs [0010] – [0011]); and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital

amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate (see Figure 1 and page 1, col. 2, paragraphs [0010] – [0011]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Matsushita-Orndorff to comprise the steps of: providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate, as taught by Midya, in order to provide error correction in digital amplifiers.

As to claim 27, Matsushita-Orndorff discloses the method according to claim 25 with keep-out bands associated with the frequency group consisting of AM, FM, and TV band frequencies ((Orndorff: see Col. 1, lines 13-15, Col. 3, lines 23-30 and Col. 4, lines 37-42). However, it does not disclose the steps of: providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate that substantially minimizes interference minimizes interference with keep-out bands. The Midya reference teaches the steps of: providing a digital amplifier having output switching responsive to the

digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate (see Figure 1 and page 1, col. 2, paragraphs [0010] – [0011]); and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate that substantially minimizes interference minimizes interference with keep-out bands (see Figure 1 and page 1, col. 2, paragraphs [0010] – [0011]).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the method of Matsushita-Orndorff to comprise the steps of: providing a digital amplifier having output switching responsive to the digital asynchronous sample rate converter output audio data and further responsive to the output audio clocks at the new sample rate; and communicating the digital asynchronous sample rate converter output audio data and the output audio clocks at the new sample rate to the digital amplifier such that the digital amplifier operates to change its output switching pulse-frame rate from a first pulse-frame rate to new pulse-frame rate that substantially minimizes interference minimizes interference with keep-out bands, as taught by Midya, in order to provide error correction in digital amplifiers.

Response to Arguments

4. Applicant's arguments filed on 12/8/04 have been fully considered but they are not persuasive.

With respect to claims 1, 12, 18 and 25, Applicant argues that Matsuhita does not disclose a controller that generates control data bits in response to user selected input frequency information or data. Applicant acknowledges that the Examiner did not rely on the Matsuhita reference for disclosing the above-cited limitation. Applicant further argues that the secondary reference, Orndorff, also does not disclose the above-cited limitation, and points only to column 3, lines 9-15 of Orndorff. Applicant concludes that nothing in Orndorff relates to frequency.

Examiner respectfully disagrees with Applicant's arguments with respect to Orndorff. In the previous Office action, Examiner relied on several portions in Orndorff in addition to the one pointed out by Applicant. For example, Orndorff states that receiver spurs are eliminated by properly selecting a second local oscillator frequency and compensating a first local oscillator frequency to avoid significant mixing products. Moreover, the selection of frequencies is performed based on a lookup table set up by a user. See col. 5, lines 43-47, col. 8, lines 12-16 and col. 11, line 59 – col. 12, line 8. Thus, contrary to Applicant's assertion, the disclosure in Orndorff does indeed relate to frequency, and the control bits generated by the controller are in response to user selected frequency information.

Conclusion

5. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after

the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Sam Bhattacharya whose telephone number is (571) 272-7917. The examiner can normally be reached on Weekdays, 9-6, with first Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lester G. Kincaid can be reached on (571) 272-7922.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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